Slip Happens: Intel Delays Merced While HP Maintains Stride

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Summary

With complex microprocessor designs, sometimes "slip happens." Delays in the development of the Merced chip – based on IA-64, which Hewlett Packard (HP) and Intel developed jointly – show that HP has played its hand wisely by maintaining an upgrade path for its PA-RISC architecture. HP plans to release the PA-8500 late in 1998 or early in 1999; the 8500 will be followed by the PA-8700 and perhaps by a further successor. HP's upgrade plan will allow its installed base to invest in PA-RISC technology without fear of losing compatibility with Merced. More importantly, the plan allows HP's customers to avoid pinning their hopes too early on Merced's yet-to-be-proven technology.

HP and Intel characterize the delay as merely a "blip" – a not-unusual schedule adjustment following reassessment of the work that remains. The intense interest in Merced forced its developers to announce target dates too early. Now Intel, HP, and their partners face scrutiny as a result of trying to estimate shipping dates years in advance. Merced's later arrival has some significant consequences: Intel must now rely on such predecessors as Xeon and Tanner to hold down the fort for an extra six months; RISC vendors who have not committed to adopting Merced now have an extra few months to match Merced's proposed performance; and companies that had depended upon Merced to jump ahead of RISC now find themselves lagging.

Early in the design process, Intel described Merced as a chip that would be second-to-none. The media, OEMs, and ISVs then created an aura for Merced that portrayed it as a RISC-killer, and Intel did little to dispel those myths. However, even if Merced's killer image proves overstated – as it now appears to be – Intel will not lose the loyal NT customers who are now running on IA-32. Nor will current customers leave Intel if the company cannot meet its self-imposed standards for Merced. The significant performance edge Merced still provides over previous Intel chip generations should appease Intel users.

On the other hand, HP has cautiously maintained that Merced will perform at the same level as other RISC chips, as was originally intended. It must continue to do so. HP was the first RISC vendor to decide that the RISC architecture would not last. It remains the largest RISC vendor moving to adopt IA-64 as its strategic architecture. (Subsequently, SGI and Siemens-Nixdorf have followed HP's lead – see page 7.)

HP has covered itself admirably in preparation for Merced by making it possible for users to move from PA-RISC to the new chip on their own timetable. If HP did not continue its PA-RISC fabrication path and Merced failed to live up to expectations, the company would stand

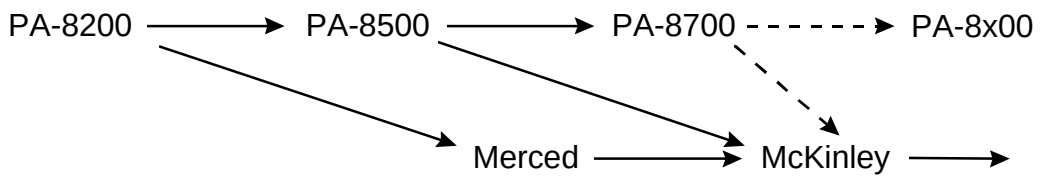
to lose not only market share, but mindshare. For this reason, HP has been cautious in extolling the virtues of Merced, preferring to remain fairly quiet until the processor ships.

HP's continuing plans for PA-RISC extend development into the early part of the next decade. The company's projected end date for PA-RISC clearly assumes that the second-generation Merced chip, code-named "McKinley," rectifies any performance deficits with the chip's initial release. If IA-64 is not a viable option for HP-UX users by then – and if future RISC outperforms EPIC – HP has a potential dilemma on its hands.

Ultimately it seems likely HP will stop PA-RISC development in 4 to 5 years for economic reasons. For any superscalar RISC vendor, both the processor design and the processor fabrication costs are enormous and rising rapidly. Intel, which can afford new fabrications, spent about $2.5 billion on its last fabrication facility. Estimates place fabrication plant costs for 2002 at about $6 billion. For this reason, Sun and SGI have historically depended on third parties for fabrication technology and focused their resources on chip design. Now the cost to design a chip that outperforms Intel has risen to well over $100 million, however, and even at that rate companies lack confidence that they can out-engineer Intel's massive investments in processor design. Because of the huge costs and low volumes associated with new chip rollouts, HP asserts the days of proprietary RISC architecture are numbered.

HP believes it will capture the lion's share of the UNIX-on-IA-64 market because of its total focus on Merced. The company believes it will fully transition its current RISC-based UNIX market share to IA-64 and will push aside the remaining RISC-based UNIX vendors who now are ignoring the IA-64 platform or addressing it only indirectly. HP estimates that vendors such as Digital and SGI will comprise only about 30 percent of the projected IA-64 market space. IBM and Sun have already stated they will not move to Merced. These projections promise 70 percent of the initial UNIX on IA-64 market share for HP-UX, potentially resulting in significant revenues for HP.

HP Prescribes Multi-Step Upgrade Path for PA-RISC



Because Merced may not offer clear performance superiority, it may not immediately appear on some HP-prescribed PA-RISC transition paths. Early adopters will be those most willing to recompile their RISC applications for optimization on the IA-64 architecture; they will

probably move to Merced as soon as it is released. For those likely to be less willing to recompile immediately, HP has designed PA-RISC system upgrade paths that will double overall performance. HP may recommend that commercial PA-8000 or PA-8200 users upgrade to PA-8500. Then commercial users can max out the PA-8500 chips in their servers before moving to IA-64 with the next-generation McKinley (slated to arrive 18 months to 2 years after Merced's initial release).

HP may not slate future PA-RISC–based servers for Merced upgrades at all. If the initial Merced chip fails to achieve its performance goals, HP's current roadmaps recommend adding more processors to these systems. If McKinley also fails to offer compelling performance advantages HP plans provide for a future PA-RISC CPU. Note that HP remains confident IA-64's growth path will quickly deliver performance at levels that will convince PA-RISC customers to move to IA-64. At the present time, though, HP has intimated that a path to Merced from the PA-8700 (which is still in the concept/design planning stages), may not provide enough of a performance boost to justify such an upgrade. In any case, HP's planned rollout of the PA-8500, PA-8700, and future PA-RISC chips will insulate the company against further Merced delays for the time being, because they ensure compatibility with IA-64 in the future.

The Merced delay may even be a blessing in disguise for HP. It means more PA-RISC users will install PA-8500 systems (slated for release at the end of this year or early next year), which are board-upgradable to Merced and will help prepare users for the IA-64 transition.

DHBA Updates Its Performance Predictions

Since DHBA's initial report on Merced in 1996,[1] Intel has upped its speed expectations for the chip. Benefiting from .18µ fabrication technology, Merced now targets over 800 MHz in the first production cycle, compared to early estimates of 400-600 MHz now being reached by the Slot 1 Pentium II and predicted for the Slot 2 Xeon (to be released early this summer). Intel expects such future releases as "Tanner" (the 1999 Slot 2 successor to Xeon) and the Slot 1 "Katmai" (expected 1Q 1999) to clock upwards of 500 MHz.[2]

The most notable change in Intel and HP's Merced strategy since DHBA's report, however, is the significantly lower performance expectations for the first IA-64–based chip. Initially, Intel touted Merced's superiority to anyone who would listen, but the company is now only cautiously optimistic. Merced should double the performance of the PA-8200, HP's current high-end RISC chip, but it may not outperform PA-RISC chips current at the time of Merced's release, in mid-2000.

Table 1: Performance Progress Report

DHBA Predictions in July 1996	Current DHBA Assessment
HP projects that its PA-RISC processors will remain among chip leaders well into 1999.	Yes – PA-8200 benchmarks rival the performance of latest UltraSPARC and Alpha chips.
The .25µ PA-8500 will double the integer performance of PA-8000 and will roll out in late 1997.	Yes – .25µ PA-8500 will double PA-8000 integer performance, although it will not arrive until 2H98.
Merced will ship in 1999.	No – Merced will ship in mid-2000.
Merced expected to target clock speeds of 400-600 MHz.	No – Instead Merced now targets a minimum clock of 800 MHz.
IA-64 architecture doubles performance at minimum and in some cases achieves 10x speedup over RISC.	Undetermined – Merced will more than double performance of mid-1996 RISC chips, but it may not outperform RISC chips current in 2000. Future IA-64 processors are expected to deliver 2x RISC performance.
HP committing staff and resources to both IA-64 and PA-8500 development to ensure it retains leadership in RISC chip performance if Merced slips.	Yes – HP developed the 8500 and will develop future PA-RISC chips. HP will make a transition from RISC to EPIC in 5 years or less.

Currently, the 236 MHz PA-8200 integer performance ranks second only to the 600 MHz Alpha. On floating-point benchmarks, the 8200 ranks second only to the IBM P2SC processor in the 397 workstation. (See Table 2.)[3]

Table 2: Current RISC Processor Performance

	HP PA-8200 236 MHz	Alpha 21164 600 MHz	UltraSPARC-II 360 MHz	IBM P2SC 160 MHz
SPECint95	17.30	18.40	16.10	8.61
SPECfp95	25.40	21.30	23.50	26.60

HP will try to ensure that it retains market share in the UNIX arena by continuing to develop its PA-RISC processor line. The PA-8500 should remain competitive among RISC vendors, with the Sun UltraSPARC-III and the Digital Alpha 21264 both slated to appear in systems within 12 months. All 3 chips should benchmark in the same general range of 30-35 integer,

50-60 floating-point. The PA-8700 remains in the concept/design phase, but may now debut about the same time as Merced. The 8700 may also outperform the first release of Merced. HP also plans a post-8700 chip for release shortly before the expected arrival of McKinley.

Migrating to Merced

Table 3: Migration Progress Table

DHBA Predictions in July 1996	Current DHBA Assessment
IA-64 represents a superset of Intel's IA-32, so Merced will run unmodified 32-bit binaries from previous Intel chips.	Mixed – IA-64 is a new instruction set architecture, not a superset of IA-32. But, the Merced implementation contains hardware to allow it to run unmodified 32-bit IA-32 binaries.
Merced will contain X86 instruction set assists to boost 16- and 32-bit application performance. Merced will not contain similar hardware assists for PA-RISC. PA-RISC apps will be dynamically reorganized using a JIT compiler to map to IA-64.	Yes – HP will rely on JIT compilers for PA-RISC binary compatibility. HP will provide compilers for critical PA-RISC applications and expects major database companies to provide Merced-optimized software for HP-UX.
Older legacy apps will be translated into native Merced binaries from PA-RISC.	Yes – Also, compilers are expected to aid this conversion if users wish to recompile.
While dynamic byte-reordering remains technically achievable in both hardware and software, performance tradeoffs remain unquantified. Lack of this ability would compromise backwards compatibility objectives when merging big-endian HP-UX and little-endian UnixWare. Users wishing to switch between little-endian UnixWare and big-endian HP-UX apps would have to reboot.	No – A merged HP-UX–UnixWare is no longer HP's strategic direction. Switching between big-endian HP-UX and little-endian NT applications will require a reboot.
HP-UX upgrade will be required to run on Merced, probably after release of HP-UX 11 in late 1997.	Yes – Minor upgrade of HP-UX 11 expected with the arrival of Merced.
Intel expects IA-32 processors to continue in mainstream with Merced and other IA-64 processors entering that range mid-2000s.	Yes – Intel plans future IA-32 processors for mainstream consumers well into the next decade, as Merced on the desktop will enter at a price premium.

To fully exploit the performance benefits of Merced, applications must be recompiled for the IA-64 instruction set. However, in some cases, recompilation may be difficult or impossible for a variety of reasons:

- Someone at the company misplaces the source code.
- The programmer who wrote the code and knows exactly how to compile it (and with which compiler tools) leaves, dies, or is fired.
- The source code is lost due to inadequate backups.
- The source code, while intact, depends on header files or shared libraries that were moved someplace else or lost.
- When moving from one chip architecture to another, differences in endian-ness or 32-64 bit word length may require source code modifications, not just a simple recompile.
- When moving from one version of the OS to another, API behavior or location of files may change in such a way that a recompile is not sufficient.

Thus, HP will enable full binary compatibility for existing PA-RISC applications on Merced through dynamic translation. When HP co-designed the IA-64 instruction set with Intel, it made sure that PA-RISC instructions mapped near 1-1 to IA-64 instructions specifically to facilitate efficient translation.

Other vendors have hinted at plans for similar schemes to move their applications from RISC to Merced, but HP claims it has an advantage because other architectures may require 2, 3, or more instructions to map their respective RISC instructions onto IA-64. At minimum, HP believes other vendors will not make dynamic translation available until some time after Merced's release. Assuming that UNIX vendors recompile their operating systems for IA-64 in time for Merced and that database vendors are persuaded to recompile for IA-64 for each UNIX, application recompilers will sort the field. Indeed, because HP's dynamic translation is so quick, HP-UX on Merced will generate IA-64 code each time it needs to run a PA-RISC application and will not store the translated code after creating it.

HP estimates commercial systems spend about 20% of their time in the operating system, 70% percent in the database, and only 10% in the application itself. By ensuring that the database and HP-UX OS are optimized for IA-64, HP can allow users to work with effectively 90% native IA-64 software even before they recompile their applications and use translation.

Intel and HP have made settling recompilation issues in time for the Merced release a high priority. Over 200 ISVs are already committed to native IA-64 versions of their applications on HP-UX. HP's strategy, as with the HP-UX 10-11 upgrade, is to make native versions of the leading databases available on IA-64 so customers will not need to upgrade to a new database version and Merced at the same time. Database upgrades will then be compatible with PA-

RISC and IA-64 when the customer migrates to Merced in the future. Indeed Merced's 6-month delay provides additional time for software to port and test to the new architecture.

SGI and Siemens-Nixdorf Propose Changes that Echo HP

SGI has planned a gradual transition strategy from MIPS to Intel similar to that of HP. SGI has yet to reveal some details of its transition, but plans to offer Intel-based NT on its entry-level workstations this fall. It will offer Intel on its midrange workstations within 2 years, running either NT or IRIX. SGI's high-end SMP workstation line and its Origin and Cray servers will gradually move to IA-64 after Merced arrives with all systems on IA-64 by 2002. Also like HP, SGI will continue with future MIPS processors until it completes that transition. SGI has finished designing and has taped out the R12000 (successor to the current R10000). It also has retained the high-end design team from MIPS to work on an R14000 product that will enhance SGI's MIPS-based solutions into the 2000-2001 timeframe.

Currently SGI does not plan to provide NT for either its server product line or its high-end SMP workstation line and will remain with IRIX UNIX. Customers moving applications from IRIX-on-MIPS to IRIX-on-Intel will need to recompile, which the company expects its largely technical customer base will find feasible. D.H. Brown Associates, Inc. (DHBA) notes with concern, however, that technical customers have grown less and less willing to recompile over time, as Sun discovered during its upgrade to Solaris.

Siemens-Nixdorf, which has also used MIPS hardware and its own operating system modified from SVR4, plans to develop a Just-In-Time compiler mechanism, Dynamic Object Code Translation, similar in concept to HP's. It will use the compiler to move its customers from MIPS to IA-64. DHBA thinks it might be sensible for SGI to look into licensing this mechanism or technology. Licensing would allow SGI to minimize its own development risk and still assist its customers with migration (perhaps not with the initial IRIX-on-IA-64 release, but at least within a year or two).

[1] See *HP's Breakout Strategy*, D.H. Brown Associates, Inc., July 1996.
[2] See an upcoming Technology Trends for an analysis of Intel's segmentation of the chip market with Xeon, Tanner, and Katmai.
[3] SPEC measure cited because no other measure of end-user, "real-world" performance was available across all chips.